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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/531,605

04/14/2005

William A Steer

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS

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BRIARCLIFF MANOR, NY 10510

EXAMINER

RAINEY, ROBERT R

ART UNIT

PAPER NUMBER

2629

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DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/531,605

Applicant(s)

STEER, WILLIAM A

Examiner

Robert R. Rainey

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 10-13 is/are rejected.
- 7) ☒ Claim(s) 1,4-10 and 14-17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 3/23/2006
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. **Claims 4-9 and 14-17** objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claims have not been further treated on the merits.
2. **Claim 10** objected to because of the following informalities: "the stored pixel drive level" has no antecedent basis in the claim. The other phrases used in the claim that seem to be related are "for storing a drive level" and "storing a pixel drive voltage". Please pick "pixel drive level", "drive level", or "pixel drive voltage" for use throughout the claim or clearly distinguish between them on the record. Appropriate correction is required. For reference note that only "pixel drive level" is associated with a drawing and "pixel drive voltage" occurs only in this claim.
3. **Claims 1 and 10** objected to because of the following informalities: In the phrase "a storage capacitor for storing a drive level and connected between an input to the pixel and the gate of the drive transistor" the "and" before "connected" seems out of place as is clear if the prepositional phrase is left out i.e. "a storage capacitor ... and connected between an input to the pixel and the gate of the drive transistor". Appropriate correction is required.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

In particular, placement of headings (f) through (j) appropriately in the specification would be helpful to future readers.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1-3 and 10-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,876,345 to *Akimoto et al.* ("*Akimoto*").

As to **claim 1**, *Akimoto* sixth embodiment discloses an active matrix electroluminescent display device comprising an array of display pixels (see for example column 5 lines 5-10 and column 1 lines 36-42), each pixel comprising: an electroluminescent display element (see for example Fig. 13 item 84 and column 12 line 35) and ; a drive transistor (see for example Fig. 13 item 91 and column 12 lines 30-36) for driving a current through the display element, a drive voltage being provided to the gate of the drive transistor (see for example Fig. 3 and column 5 lines 40-42, which generally teaches to V_{in} to V_{out} relationship); and a storage capacitor (see for example Fig. 13 item 82 and column 12 lines 25-30) for storing a drive level (see for example "signal voltage" of Fig. 14 and column 12 lines 51-55) and connected between an input to the pixel and the gate of the drive transistor (see for example Fig. 13, which shows capacitor 82 so connected), wherein driver circuitry is provided for providing a linear voltage waveform to the input of the pixel (see for example Fig. 14 "PIXEL DRIVING VOLTAGE" associated with "DRIVING SIGNAL LINE" and column 12 lines 55-60), the voltage waveform being voltage-shifted by the storage capacitor before

application to the gate of the drive transistor (see for example Fig. 13 and column 12 lines 51-60, which describe the storage of a signal voltage on the capacitor followed by the application of a triangular waveform to the capacitor through line 96; this results in the triangular waveform being voltage-shifted by the amount of the stored signal voltage before being applied to the gate of the drive transistor).

Akimoto sixth embodiment does not expressly disclose that the voltage waveform is stepped or that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor.

Akimoto third embodiment discloses that the voltage waveform is stepped and that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of an inverter (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter is off at one step and on at another).

Akimoto sixth embodiment and *Akimoto* third embodiment are analogous art because they are from the same field of endeavor, which is image displays capable of multilevel display, and seek to solve the same problem, which is to reduce the variation in PWM circuits caused by differences between TFT circuitry.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the stepped waveform of *Akimoto* third embodiment to the circuit of *Akimoto* sixth embodiment. The

suggestion/motivation would have been to provide advantages such as to prevent changes caused by noise (see for example column 10 lines 11-14).

Akimoto sixth embodiment as modified by *Akimoto* third embodiment disclose the claimed invention except for the height of the steps in the stepped voltage waveform being greater than the voltage width of the linear operating region of the drive transistor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to set the step height sufficiently large to ensure that the transistor was fully on or fully off as was the case for the inverter of *Akimoto* third embodiment, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272,205 USPQ 215 (CCPA 1980).

As to **claim 2**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment:

Akimoto sixth embodiment and *Akimoto* third embodiment do not expressly disclose that the height of the steps in the stepped voltage waveform is sufficient to include the linear operating region voltages of the drive transistors of all pixels of the display.

Akimoto sixth embodiment as modified by *Akimoto* third embodiment disclose the claimed invention except for the height of the steps in the stepped voltage waveform being sufficient to include the linear operating region voltages of the drive transistors of all pixels of the display. It would have been obvious to

one having ordinary skill in the art at the time the invention was made to set the step height sufficiently large to ensure that all transistors were fully on or fully off as was the case for the inverters of *Akimoto* third embodiment, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272,205 USPQ 215 (CCPA 1980).

As to **claim 3**, in addition to the rejection of claim 1 or claim 2 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third embodiment further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any input voltage for the inverter in the linear region corresponds to a voltage between steps of the voltage applied to the input of the inverter (see for example column 10 lines 15-21, especially noting that the steps are chosen large enough that noise would not cause the output to shift from one state to another, and Fig. 10, which shows two different stored levels, and that these levels are set at the midpoint between step levels).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to select drive levels to ensure that the linear region of the drive transistor of *Akimoto* sixth embodiment fell between steps as was ensured for the linear region of the inverter by the selection of drive levels in *Akimoto* third embodiment.

As to **claim 10**, *Akimoto* sixth embodiment discloses a method of addressing an active matrix electroluminescent display device comprising an array of display pixels (see for example column 5 lines 5-10 and column 1 lines 36-42), each pixel comprising: an electroluminescent display element (see for example Fig. 13 item 84 and column 12 line 35) and ; a drive transistor (see for example Fig. 13 item 91 and column 12 lines 30-36) for driving a current through the display element, a drive voltage being provided to the gate of the drive transistor (see for example Fig. 3 and column 5 lines 40-42, which generally teaches to V_{in} to V_{out} relationship); and a storage capacitor (see for example Fig. 13 item 82 and column 12 lines 25-30) for storing a drive level (see for example "signal voltage" of Fig. 14 and column 12 lines 51-55) and connected between an input to the pixel and the gate of the drive transistor (see for example Fig. 13, which shows capacitor 82 so connected), the method comprising, for each pixel: storing a pixel drive voltage on the storage capacitor (see for example "signal voltage" of Fig. 14 and column 12 lines 51-55); providing a linear ramp waveform to the input of the pixel (see for example Fig. 14 "PIXEL DRIVING VOLTAGE" associated with "DRIVING SIGNAL LINE" and column 12 lines 55-60), the linear ramp waveform being voltage-shifted by the storage capacitor before application to the gate of the drive transistor (see for example Fig. 13 and column 12 lines 51-60, which describe the storage of a signal voltage on the capacitor followed by the application of a triangular waveform to the capacitor through line 96; this results in the triangular waveform being voltage-shifted by

the amount of the stored signal voltage before being applied to the gate of the drive transistor), such that for a first portion of the voltage ramp applied to the gate of the drive transistor, the drive transistor is turned on (see for example Fig. 5 "ILLUMINATING PERIOD"), and for a second portion of the voltage ramp applied to the gate of the drive transistor, the drive transistor is turned off (see for example Fig. 5 the portion of the ramp not part of the "ILLUMINATING PERIOD"), the first and second portions being determined by the stored pixel drive level (see for example Fig. 5 in which the "SIGNAL VOLTAGE" level determines the switch point).

Akimoto sixth embodiment does not expressly disclose that the voltage waveform is stepped and the on and off portions consisting of first and second sets of steps respectively.

Akimoto third embodiment discloses that the voltage waveform is stepped and the on and off portions consisting of first and second sets of steps respectively (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter is on for period corresponding to a first set of steps indicated as being part of the "COLUMN ILLUMINATING PERIOD" and off for the rest or second set of steps).

Akimoto sixth embodiment and *Akimoto* third embodiment are analogous art because they are from the same field of endeavor, which is image displays capable of multilevel display, and seek to solve the same problem, which is to

reduce the variation in PWM circuits caused by differences between TFT circuitry.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the stepped waveform of *Akimoto* third embodiment to the circuit of *Akimoto* sixth embodiment. The suggestion/motivation would have been to provide advantages such as to prevent changes caused by noise (see for example column 10 lines 11-14).

As to **claim 11**, in addition to the rejection of claim 10 over *Akimoto* sixth embodiment and *Akimoto* third embodiment:

Akimoto sixth embodiment and *Akimoto* third embodiment do not expressly disclose that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor.

Akimoto sixth embodiment as modified by *Akimoto* third embodiment disclose the claimed invention except for the height of the steps in the stepped voltage waveform being greater than the voltage width of the linear operating region of the drive transistor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to set the step height sufficiently large to ensure that the transistor was fully on or fully off as was the case for the inverter of *Akimoto* third embodiment, since it has been held that

discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272,205 USPQ 215 (CCPA 1980).

As to **claim 12**, in addition to the rejection of claim 11 over *Akimoto* sixth embodiment and *Akimoto* third embodiment:

Akimoto sixth embodiment and *Akimoto* third embodiment do not expressly disclose that the height of the steps in the stepped voltage waveform is greater than the voltage width of the overlaid linear operating region voltages of the drive transistors of all pixels of the display.

Akimoto sixth embodiment as modified by *Akimoto* third embodiment disclose the claimed invention except for the height of the steps in the stepped voltage waveform being greater than the voltage width of the overlaid linear operating region voltages of the drive transistors of all pixels of the display. It would have been obvious to one having ordinary skill in the art at the time the invention was made to set the step height sufficiently large to ensure that all transistors were fully on or fully off as was the case for the inverters of *Akimoto* third embodiment, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272,205 USPQ 215 (CCPA 1980).

As to **claim 13**, in addition to the rejection of claim 10 or 11 or 12 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third

embodiment further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any input voltage for the inverter in the linear region corresponds to a voltage between steps of the voltage applied to the input of the inverter (see for example column 10 lines 15-21, especially noting that the steps are chosen large enough that noise would not cause the output to shift from one state to another, and Fig. 10, which shows two different stored levels, and that these levels are set at the midpoint between step levels).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to select drive levels to ensure that the linear region of the drive transistor of *Akimoto* sixth embodiment fell between steps as was ensured for the linear region of the inverter by the selection of drive levels in *Akimoto* third embodiment.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. 6,809,710 to Prache et al. discloses a stored voltage modifying a ramped voltage. Corresponds to WO0154107 cited on IDS.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert R. Rainey whose telephone number is (571)

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270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/


AMARE MENGISTU
SUPERVISORY PATENT EXAMINER